AMENDMENTS TO THE CLAIMS:

Please cancel claim 38, without prejudice or disclaimer of its subject matter, and amend claim 39 as indicated below. This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1.-29. (Canceled)

30. (Previously Presented) A semiconductor device comprising:

a substrate;

a device isolation insulating film formed on one major surface of said substrate,

a gate electrode formed on the major surface of said substrate;

a gate wiring layer formed in said device isolation insulating film and connected to said gate electrode;

a source electrode and drain electrode arranged on the major surface of said substrate to face each other via said gate electrode; and

an insulating film covering bottom and side surfaces of each of said gate electrode and said gate wiring layer; and

wherein said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film.

31. (Previously Presented) A device according to claim 30, further comprising a source diffusion layer and a drain diffusion layer below said source electrode and said drain electrode.

32. (Original) A device according to claim 31, wherein said gate electrode and said gate wiring layer have bottom surfaces lower than upper surfaces of said source and drain diffusion layers.

33. (Original) A device according to claim 30, wherein said gate electrode, said gate wiring layer, and said source and drain electrodes have upper surface levels equal to each other.

34. (Original) A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels lower than upper surface levels of said source and drain electrodes.

35. (Original) A device according to claim 30, wherein said gate electrode and said gate wiring layer have upper surface levels higher than upper surface levels of said source and drain electrodes.

36. (Previously Presented) A device according to claim 30, further comprising a connection wiring layer connected to at least one of said source electrode, said drain electrode, said gate electrode, and said gate wiring layer, said connection wiring layer having an upper surface level equal to or lower than the upper surface level of said device isolation insulating film.

37. (Previously Presented) A semiconductor device comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer;

a pair of thin films formed on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator, wherein a region of said pair of thin films between said gate sidewall and said substrate contains a semiconductor and a conductive impurity, and wherein the region of said pair of thin films between said gate sidewall and said substrate has an upper surface level higher than an upper surface level of a portion of the substrate below the gate wiring layer.

38. (Canceled)

39. (Currently Amended) A semiconductor device ~~according to claim 38~~ comprising:

a substrate;

a gate wiring layer formed on one major surface of said substrate;

an insulating film interposed between said substrate and said gate wiring layer and covering a side surface of said gate wiring layer;

a pair of thin films formed on one major surface of said substrate, and arranged on two sides of said gate wiring layer; and

a gate sidewall formed on said pair of thin films, covering said side surface of said gate wiring layer, and made of an insulator, wherein a region of said pair of thin films between said gate sidewall and said substrate, a remaining region of said pair of thin films on which said gate sidewall is absent, and a surface region of said substrate in contact with the remaining region contain a semiconductor and a conductive impurity,

wherein the region of said pair of thin films between said gate sidewall and said substrate has an upper surface level higher than an upper surface level of a portion of the substrate below the gate wiring layer.